



MK6601

Complementary Enhancement Mode Field Effect Transistor

N-Channel

V(BR)DSS	RDS(on)MAX	ID
30 V	60mΩ@ 10V	4A
	75mΩ@ 4.5V	
	115mΩ@ 2.5V	

P-Channel

V(BR)DSS	RDS(on)MAX	ID
-30	120mΩ@ -10V	-4A
	170mΩ@ -4.5V	
	250mΩ@ -2.5V	

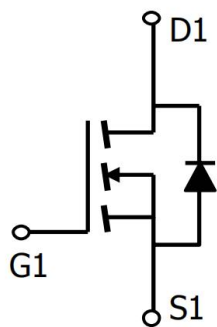
FEATURE:

※ TrenchFET Power MOSFET

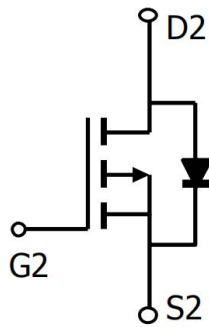
MARKING:

F1PA-MK

Equivalent Circuit:



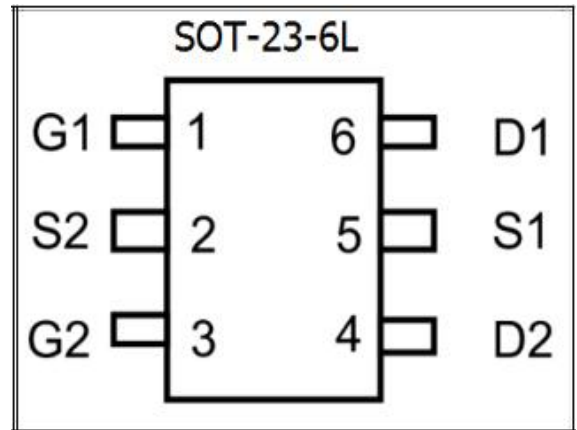
n-channel



p-channel

General Description:

The MK6601 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications. Standard Product MK6601 is Pb-free (meets ROHS & Sony 259 specifications).



Maximum ratings (Ta=25°C unless otherwise noted)

Parameter	Symbol	Max n-channel	Max P-channel	Unit
Drain-Source Voltage	VDS	30	-30	V
Gate-Source Voltage	VGS	±12	±12	
Continuous Drain Current	ID	4	-4	A
Pulsed Diode Curren	IDM	30	-30	
Continuous Source-Drain Current(Diode Conduction)	IS	1.5	-1.3	
Power Dissipation	PD	1.15	1.15	W
Thermal Resistance from Junction to Ambient (t≤10s)	RθJA	125	125	°C/W
Operating Junction	TJ	150	150	°C
Storage Temperature	TSTG	-55~+150	-55~+150	°C



N-channel

N-channel MOSFET Electrical Characteristics (Ta = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-source breakdown voltage	V(BR)DSS	VGS = 0V, ID = 250μA	30			V
Gate-source threshold voltage	VGS(th)	VDS =VGS, ID = 250μA	0.6		1.4	V
Gate-body leakage current	IGSS	VDS =0V, VGS = ±12V			±100	nA
Zero gate voltage drain current	IDSS	VDS = 30V, VGS =0V			1	μA
Static Drain-Source On-Resistance	RDS(on)	VGS = 10V, ID = 3.4A		50	60	mΩ
		VGS = 4.5V, ID = 3A		60	75	mΩ
		VGS = 2.5V, ID = 2.8A		88	115	mΩ
Forward transconductance	gfs	VDS = 5V, ID = 4A		8		S
Diode forward voltage	VSD	IS= 1A,VGS=0V		0.8	1.3	V
Maximum Body-Diode Continuous Current	IS				1.5	A
Dynamic						
Input capacitance	Ciss	VDS = 15V, VGS =0V, f=1MHz		390		pF
Output capacitance	Coss			54.5		pF
Reverse transfer capacitance	Crss			41		pF
Total gate charge	Qg	VDS = 15V, VGS = 10V, ID =4A		4.5		nC
Gate-source charge	Qgs			1.4		nC
Gate-drain charge	Qgd			0.6		nC
Gate resistance	Rg	f=1MHz		3		Ω
Switching						
Turn-on delay time	td(on)	VDS= 15V RL=5Ω, ID =4A, VGS= 10V,Rg=6Ω		4		ns
Rise time	tr			2		ns
Turn-off delay time	td(off)			22		ns
Fall time	tf			3		ns
Body Diode Reverse Recovery Time	Trr	IF=4A, dI/dt=100A/μs		11		ns
Body Diode Reverse Recovery Charge	Qrr	IF=4A, dI/dt=100A/μs		5.5		nC

Note :

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t < 10 sec.
3. Pulse Test : Pulse Width≤300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.



P-channel

P-channel MOSFET Electrical Characteristics (Ta = 25 °C Unless Otherwise Noted)

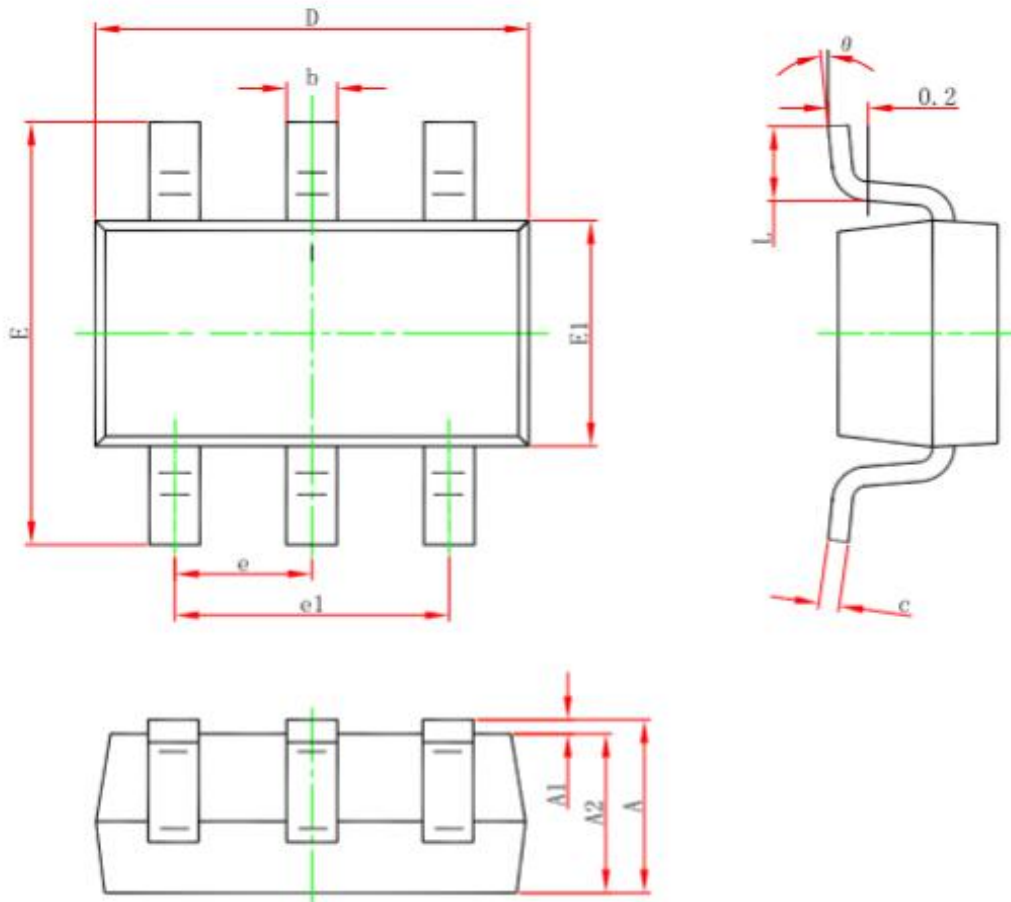
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-source breakdown voltage	V(BR)DSS	VGS = 0V, ID = -250μA	-30			V
Gate-source threshold voltage	VGS(th)	VDS =VGS, ID = -250μA	-0.6		-1.4	V
Gate-body leakage current	IGSS	VDS =0V, VGS = ±12V			±100	nA
Zero gate voltage drain current	IDSS	VDS = -24V, VGS =0V			-1	μA
Static Drain-Source On-Resistance	RDS(on)	VGS = -10V, ID = -2.5A		107	120	mΩ
		VGS = -4.5V, ID = -2A		135	170	mΩ
		VGS = -2.5V, ID = 1A		195	250	mΩ
Forward transconductance	gfs	VDS = -5V, ID = -4A		8		S
Diode forward voltage	VSD	IS= -1A,VGS=0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	IS				-1.4	A
Dynamic						
Input capacitance	Ciss	VDS = -15V, VGS =0V, f=1MHz		409		pF
Output capacitance	Coss			55		pF
Reverse transfer capacitance	Crss			42		pF
Total gate charge	Qg	VDS = -15V, VGS = -10V, ID = -4A		4.8		nC
Gate-source charge	Qgs			1.4		nC
Gate-drain charge	Qgd			0.72		nC
Gate resistance	Rg	f=1MHz		12		Ω
Switchingb						
Turn-on delay time	td(on)	VDS= -15V RL= 4.4Ω, ID = -4A, VGS= -10V,Rg=3Ω		13		ns
Rise time	tr			10		ns
Turn-off delay time	td(off)			28		ns
Fall time	tf			13		ns
Body Diode Reverse Recovery Time	Trr	IF= -4A, dI/dt=100A/μs		26		ns
Body Diode Reverse Recovery Charge	Qrr	IF= -4A, dI/dt=100A/μs		15.6		nC

Note :

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t < 10 sec.
3. Pulse Test : Pulse Width≤300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.



SOT-23-6L PACKAGE OUTLINE DIMENSIONS:



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°



N-channel Typical Electrical AND Thermal Characteristics:

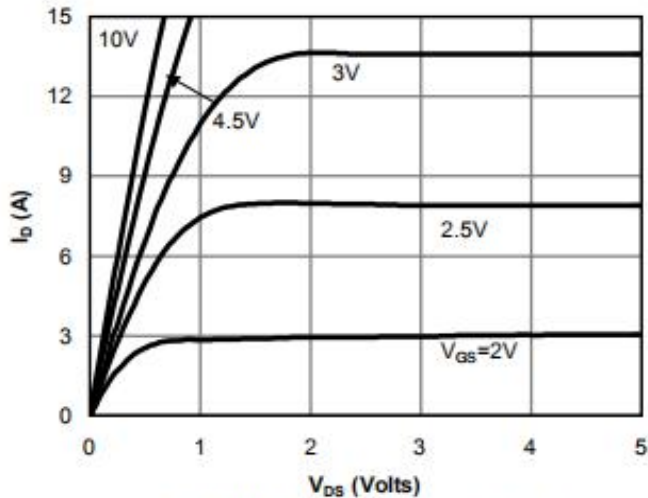


Fig 1: On-Region Characteristics

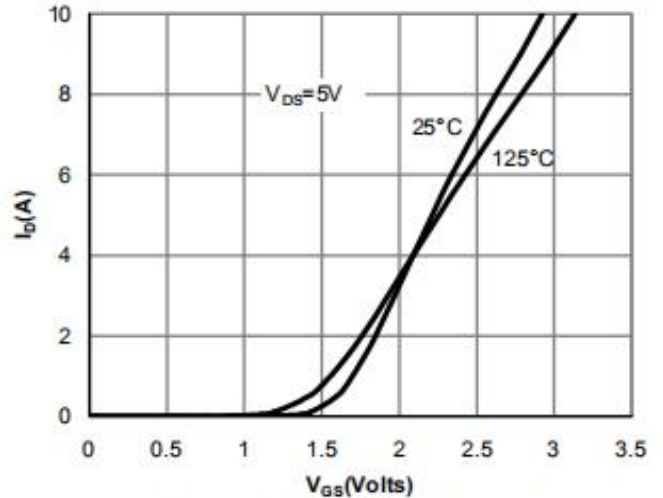


Figure 2: Transfer Characteristics

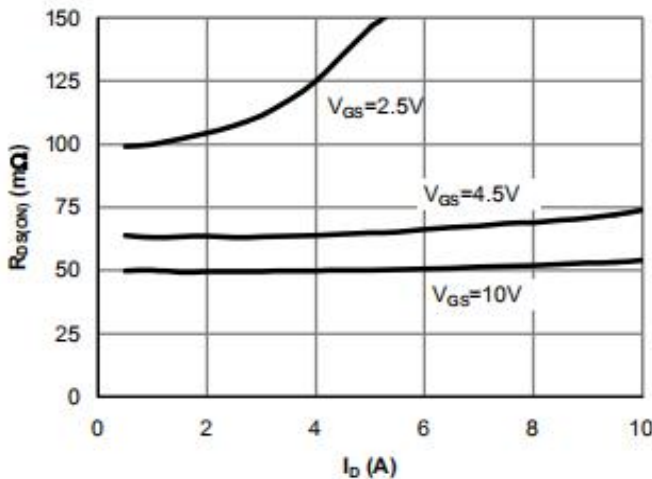


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

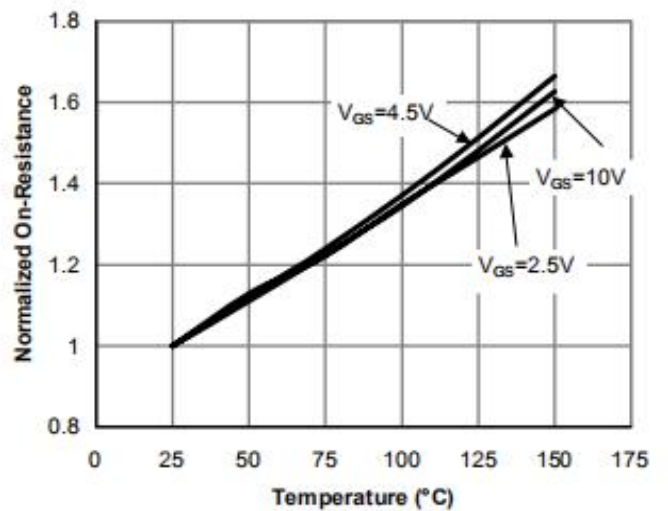


Figure 4: On-Resistance vs. Junction Temperature

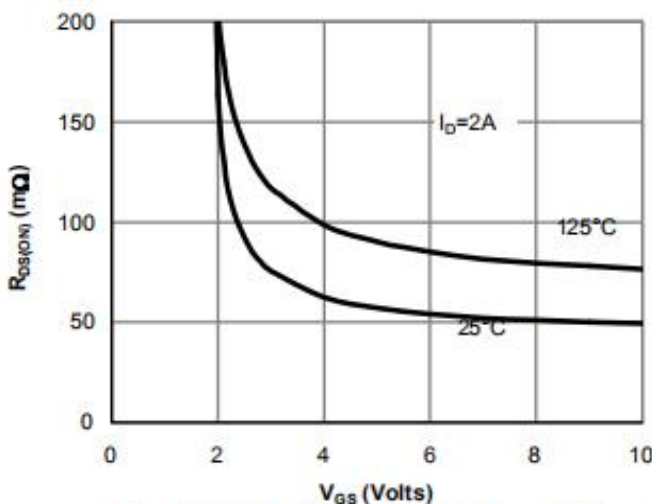


Figure 5: On-Resistance vs. Gate-Source Voltage

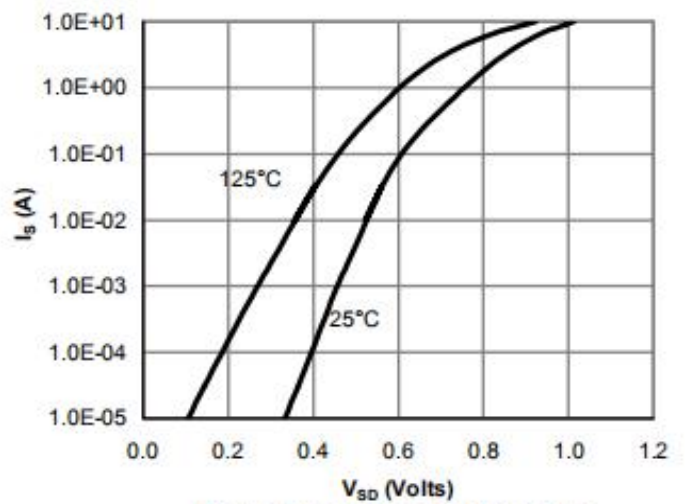


Figure 6: Body-Diode Characteristics



N-channel Typical Electrical AND Thermal Characteristics:

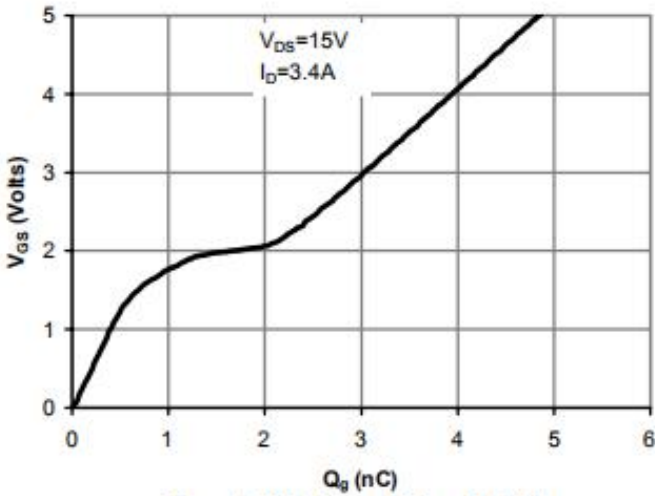


Figure 7: Gate-Charge Characteristics

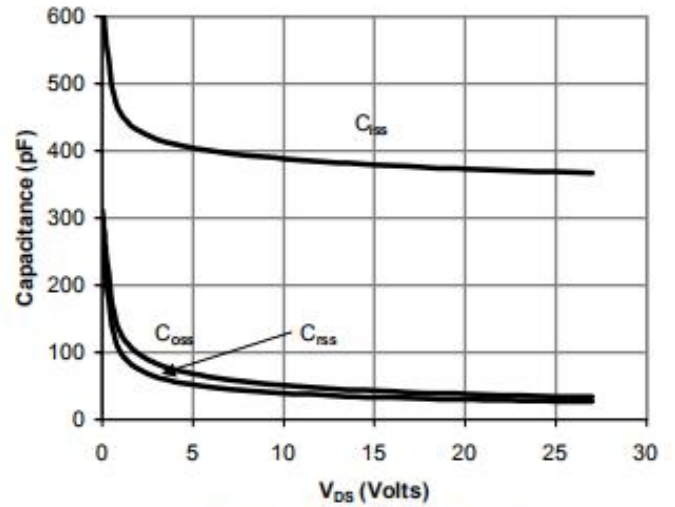


Figure 8: Capacitance Characteristics

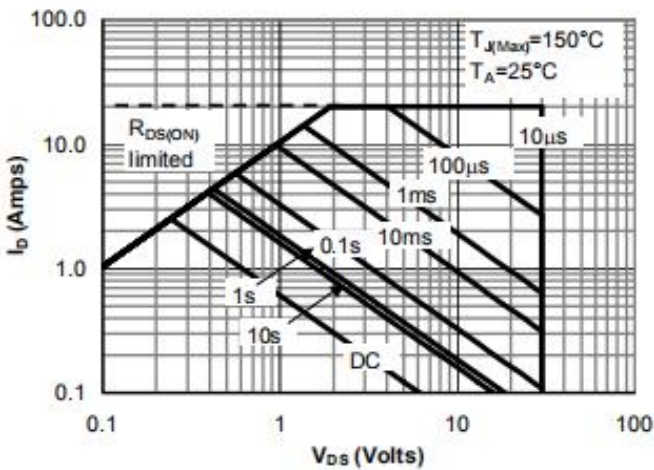


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

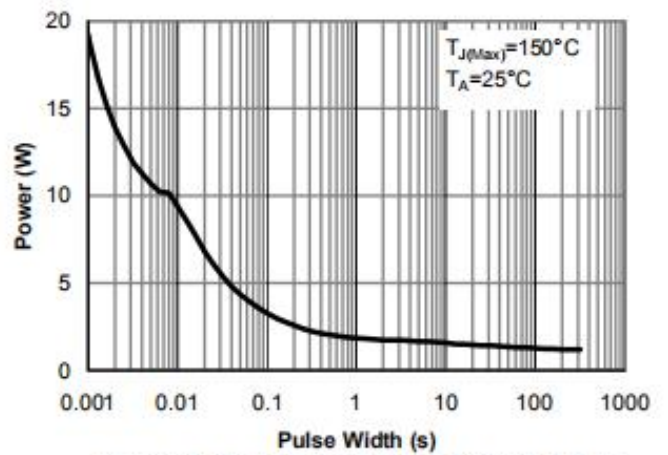


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

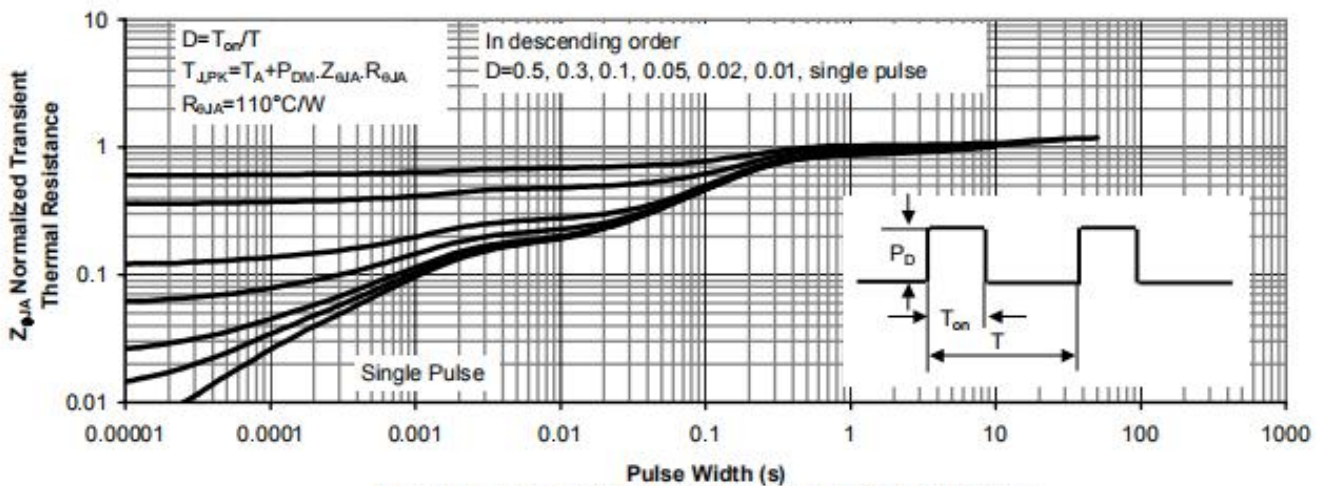


Figure 11: Normalized Maximum Transient Thermal Impedance



P-channel Typical Electrical AND Thermal Characteristics:

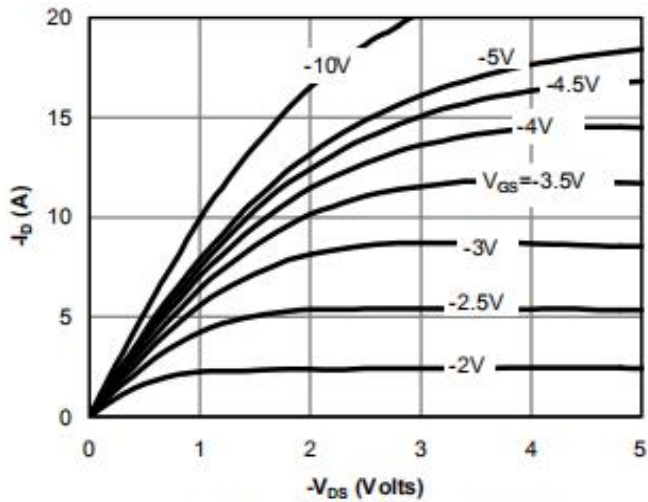


Fig 1: On-Region Characteristics

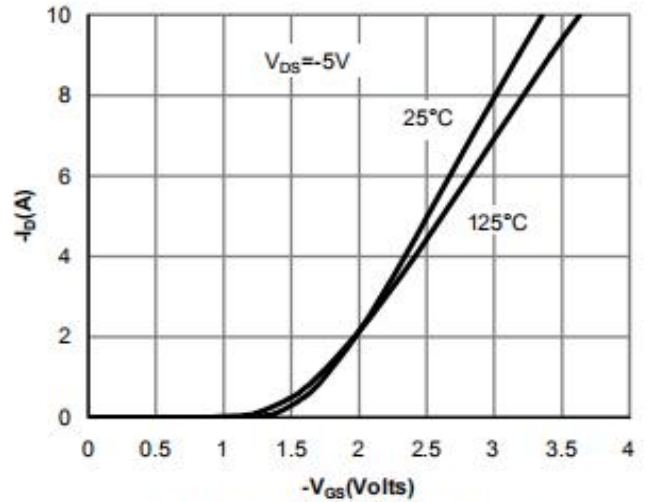


Figure 2: Transfer Characteristics

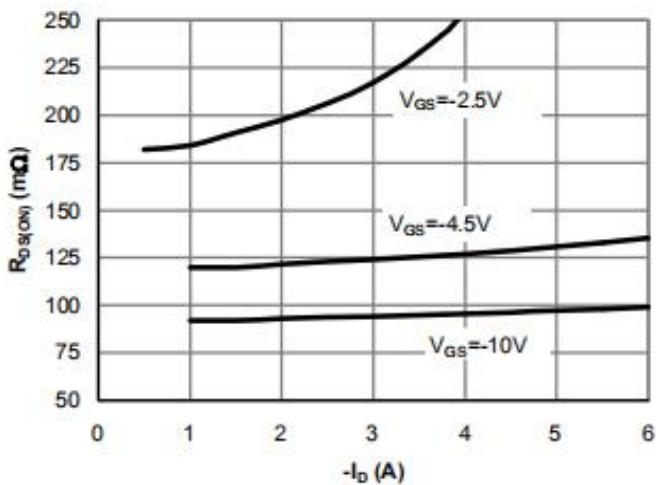


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

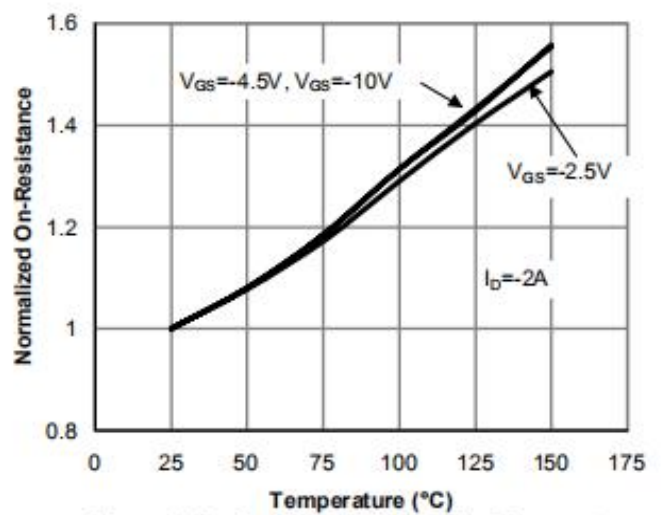


Figure 4: On-Resistance vs. Junction Temperature

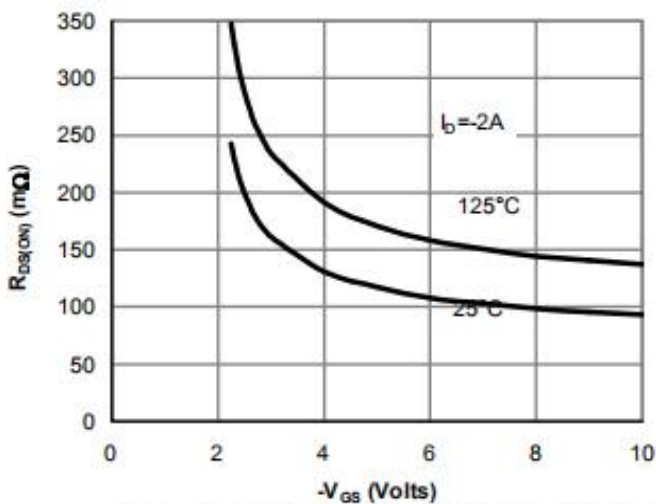


Figure 5: On-Resistance vs. Gate-Source Voltage

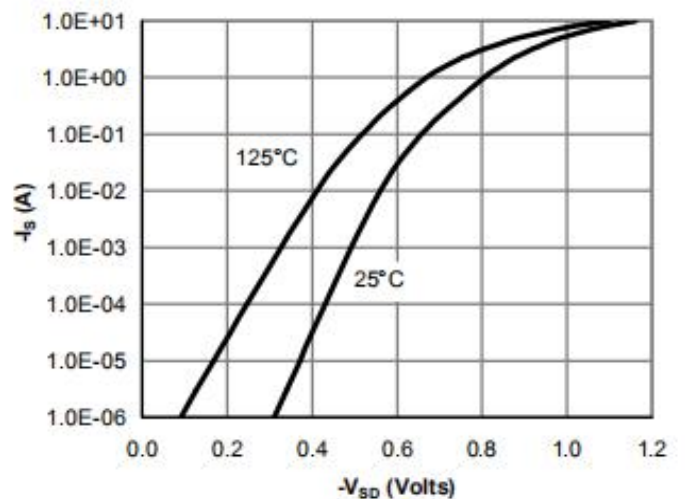


Figure 6: Body-Diode Characteristics



P-channel Typical Electrical AND Thermal Characteristics:

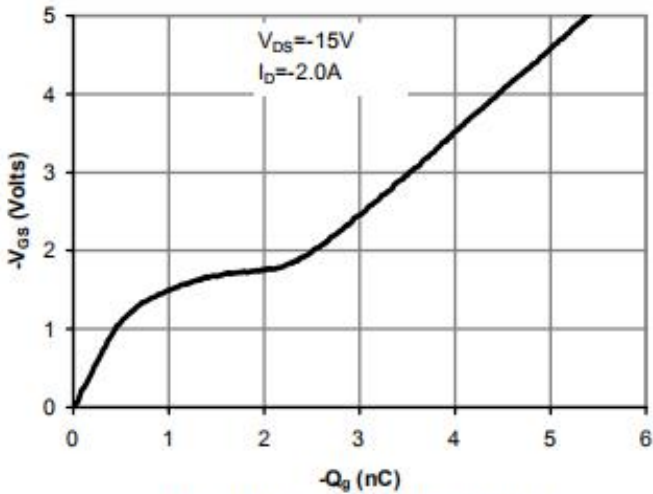


Figure 7: Gate-Charge Characteristics

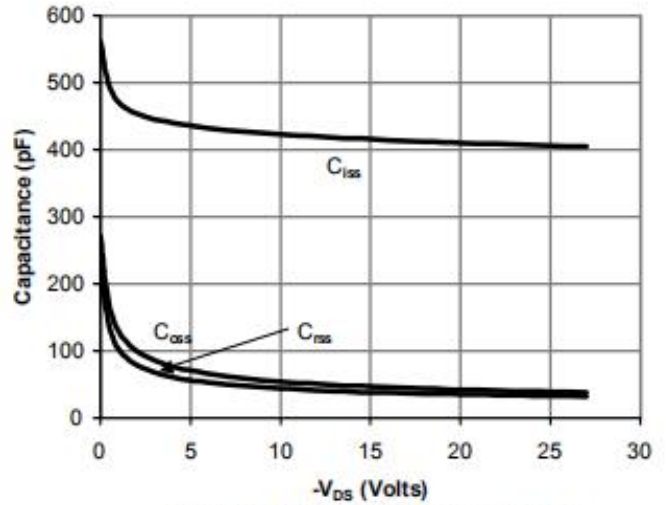


Figure 8: Capacitance Characteristics

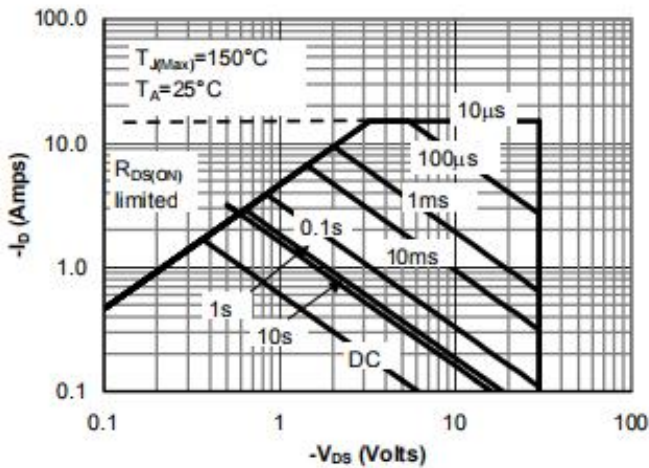


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

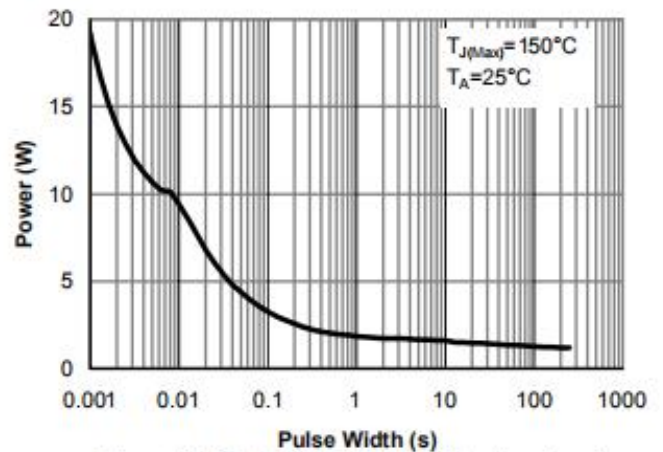


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

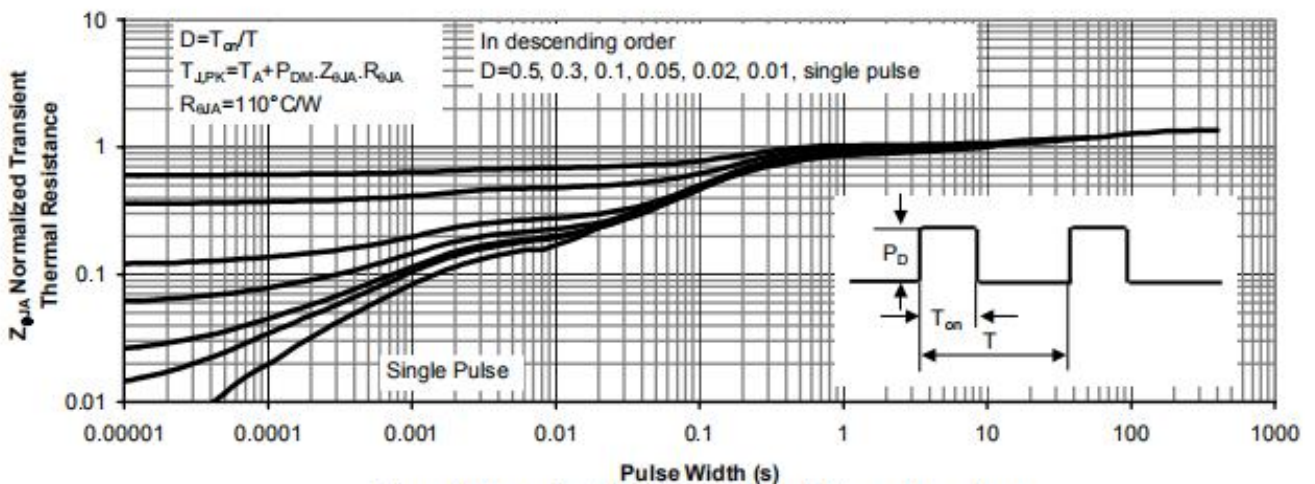


Figure 11: Normalized Maximum Transient Thermal Impedance