SHENZHEN MENGKE ELECTRONICS TECHNOLOGY CO.,LTD

SOT-23-6L Plastic-Encapsulate MOSFETS

NDC7002N Dual N-Channel 50-V(D-S) MOSFET

V(BR)DSS	RDS(on)MAX	ID
50 V	3Ω @ 10V	0.51A
	4Ω @ 4.5V	

FEATURE:

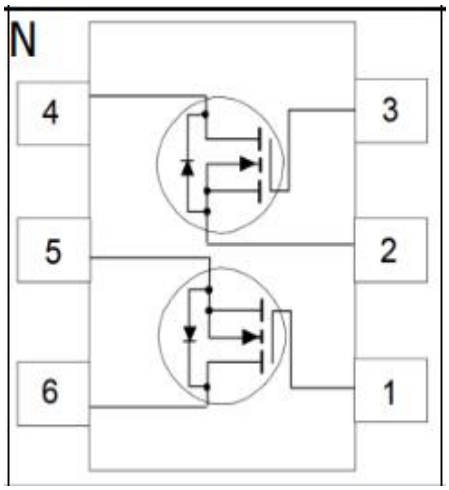
- High density cell design for low RDS(ON)
- High saturation current

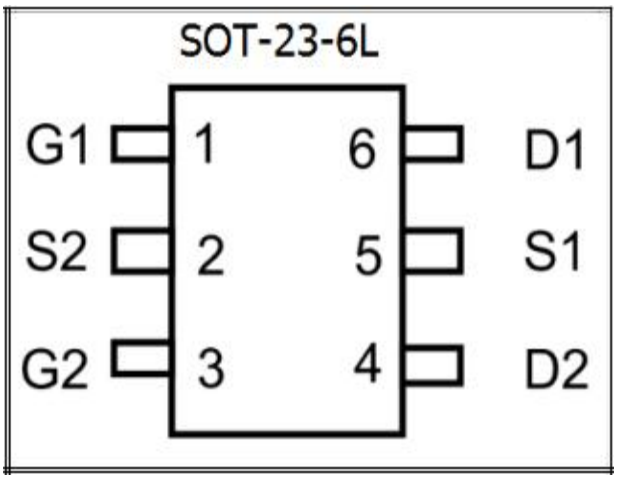
MARKING: **02Nf**

General Description:

These Dual N-Channel enhancement mode power fieldeffect transistors are produced using Fairchild'sproprietary, high cell density, DMOS technology. Thisvery high density process has been designed to minimizeon-state resistance, provide rugged and reliableperformance and fast switching. These devices isparticularly suited for low voltage applications requiring alow current high side switch.

Equivalent Circuit:





Maximum ratings (Ta=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	VDS	50	V
Gate-Source Voltage	VGS	±20	
Continuous Drain Current	ID	0.51	A
Pulsed Diode Curren	IDM	1.5	
Continuous Source-Drain Current(Diode Conduction)	IS	1.5	
Power Dissipation	PD	0.96	W
Thermal Resistance from Junction to Ambient (t≤10s)	RθJA	130	℃/W
Operating Junction	TJ	150	℃
Storage Temperature	TSTG	-55~+150	℃

MOSFET ELECTRICAL CHARACTERISTICS

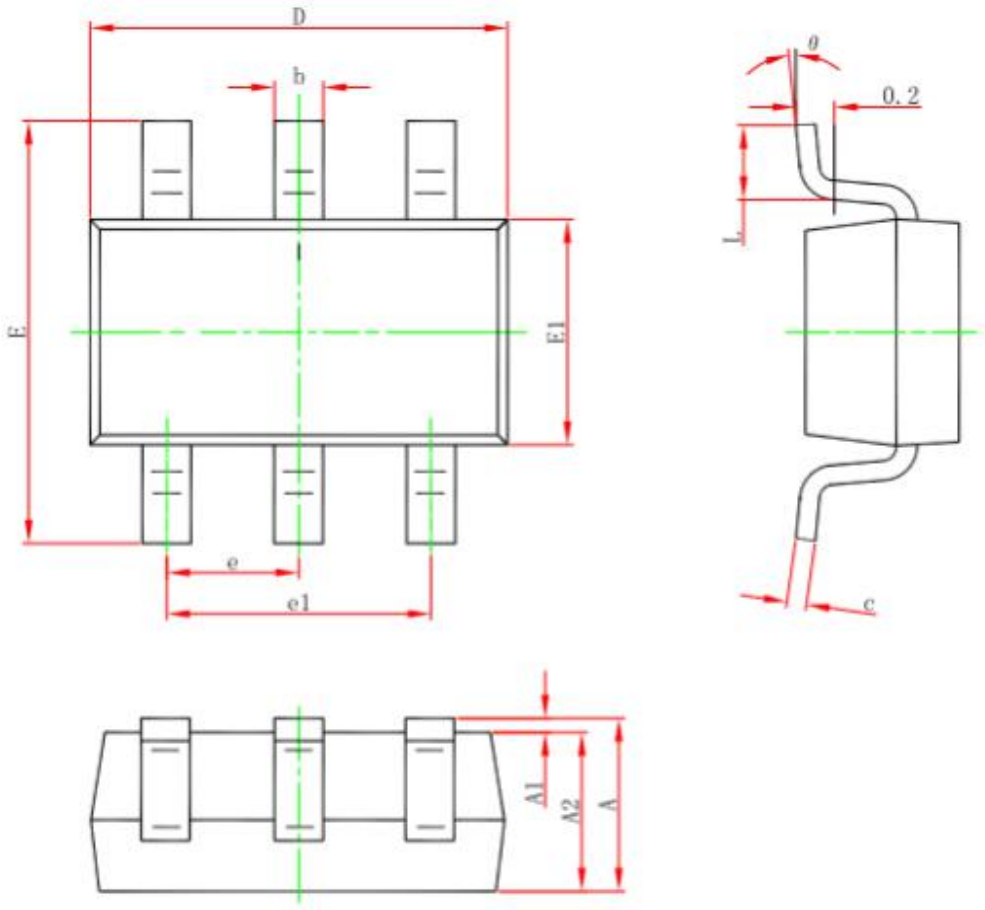
Static Electrical Characteristics (Ta = 25 ℃ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-source breakdown voltage	V(BR)DSS	VGS = 0V, ID = 250μA	50			V
Gate-source threshold voltage	VGS(th)	VDS =VGS, ID = 250μA	1		2.5	V
Gate-body leakage current	IGSS	VDS =0V, VGS = ±20V			±100	nA
Zero gate voltage drain current	IDSS	VDS = 48V, VGS =0V			1	μA
Static Drain-Source On-Resistance	RDS(on)	VGS = 10V, ID = 0.51A		1	3	Ω
		VGS = 4.5V, ID = 0.35A		1.25	4	Ω
Forward transconductancea	gfs	VDS = 5V, ID = 3.4A		400		mS
Diode forward voltage	VSD	IS= 1A,VGS=0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	IS				0.51	A
Dynamic						
Input capacitance	Ciss	VDS = 25V, VGS =0V, f=1MHz		20		pF
Output capacitance	Coss			13		pF
Reverse transfer capacitanceb	Crss			5		pF
Total gate charge	Qg	VDS = 25V, VGS = 10V, ID =0.51A		1		nC
Gate-source charge	Qgs			0.19		nC
Gate-drain charge	Qgd			0.33		nC
Switchingb						
Turn-on delay time	td(on)	VDS= 25V RL=4.4Ω, ID =0.25A, VGS= 10V,Rg=3Ω		6	20	ns
Rise time	tr			6	20	ns
Turn-off delay time	td(off)			11	20	ns
Fall time	tf			5	20	ns

Note :

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t < 10 sec.
3. Pulse Test : Pulse Width≤300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

SOT-23-6L PACKAGE OUTLINE DIMENSIONS:



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Typical Electrical Thermal Characteristics:

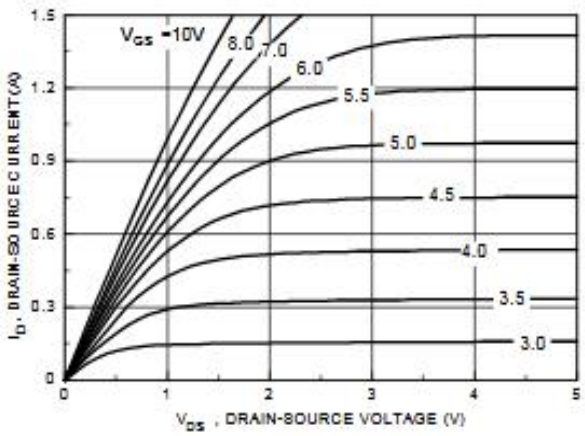


Figure 1. On-Region Characteristics.

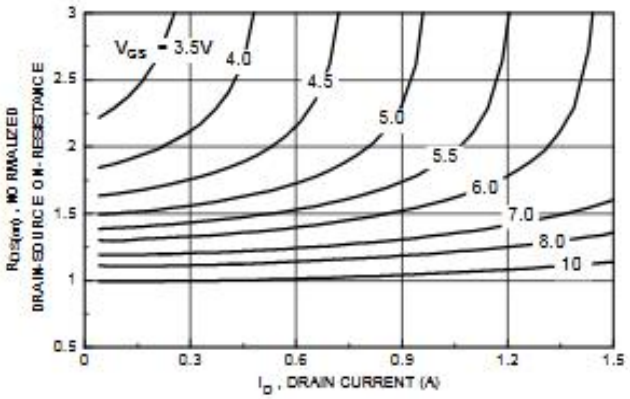


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

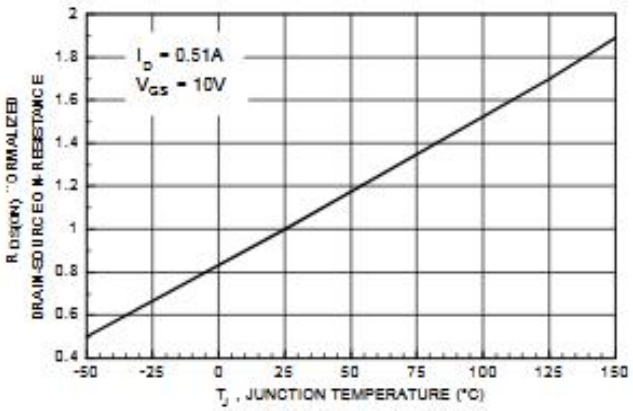


Figure 3. On-Resistance Variation with Temperature.

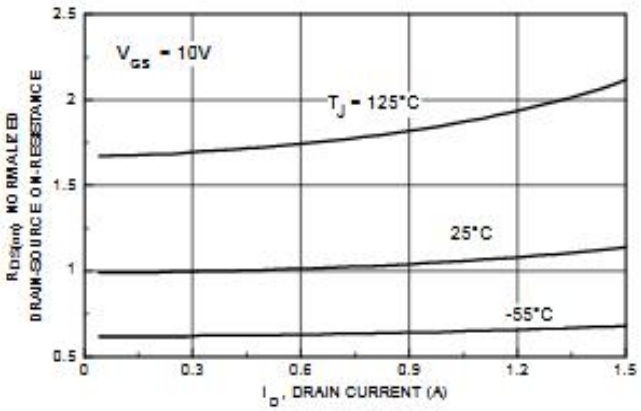


Figure 4. On-Resistance Variation with Drain Current and Temperature.

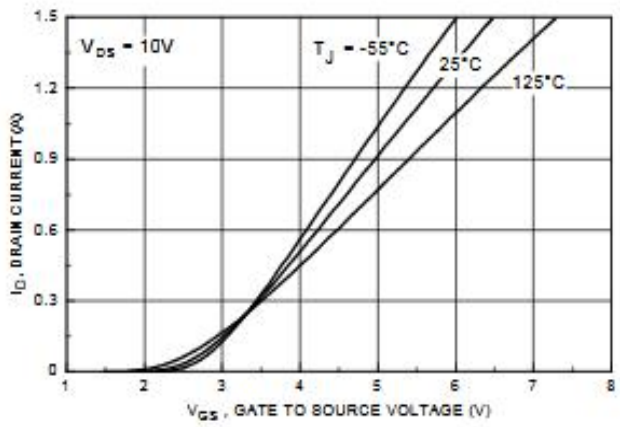


Figure 5. Transfer Characteristics.

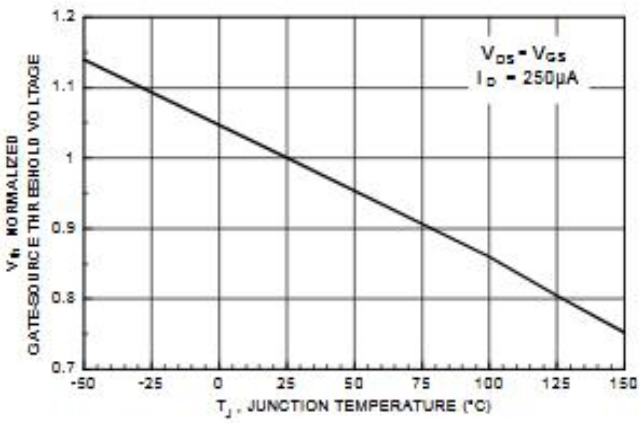


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Thermal Characteristics:

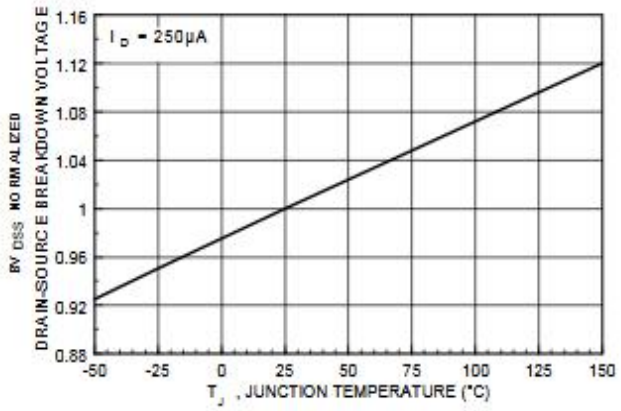


Figure 7. Breakdown Voltage Variation with Temperature.

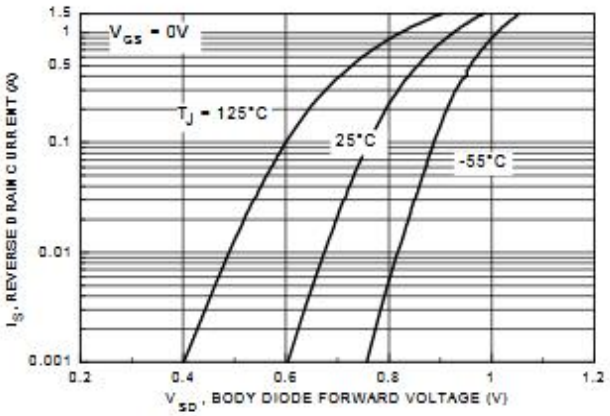


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

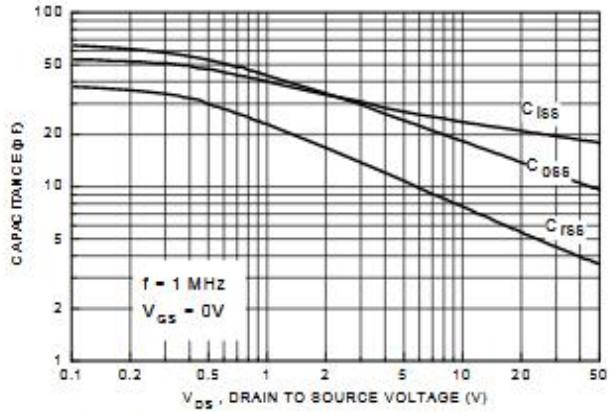


Figure 9. Capacitance Characteristics.

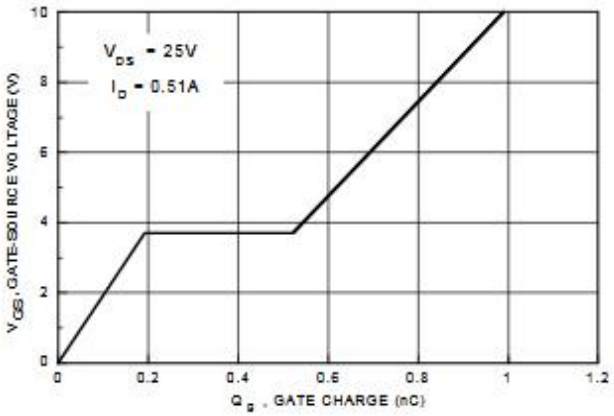


Figure 10. Gate Charge Characteristics.

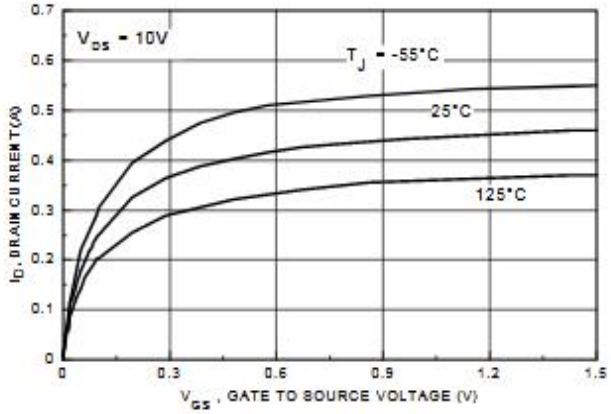


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Electrical Thermal Characteristics:

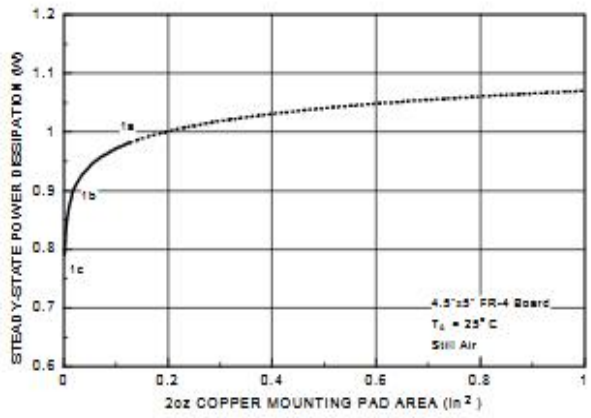


Figure 12. SOT-6 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

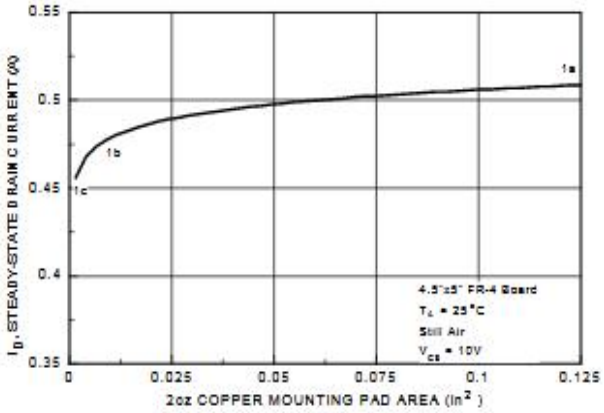


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

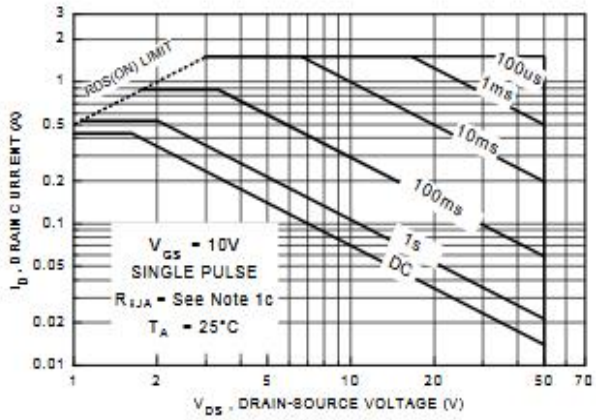


Figure 14. Maximum Safe Operating Area.

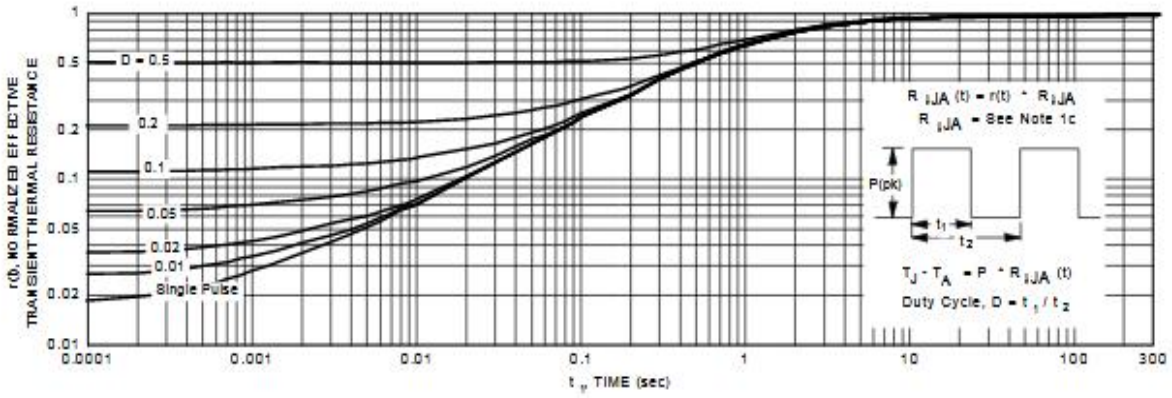


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.